

-REMARKS-

This paper is responsive to an Official Action that issued in this case on October 28, 2002. In that Action, the Office:

- finalized its restriction requirement, withdrawing claims 1-8 from consideration;
- rejected claims 16-19 under 35 USC §102 as anticipated by U.S. Pat. No. 5,327,327 to Frew et al.; and
- rejected claims 9-15 under 35 USC §103 as being obvious over Frew et al. in view of U.S. Pat. No. 5,925,725 to Ball.

Claims 1-19 are in the case.

Claims 16-19 are Not
Anticipated by Frew et al.

The Office alleged that claims 16-19 are anticipated by Frew et al. Independent claim 16 recites an article that comprises, in pertinent part:

a plurality of integrated circuit ("IC") chips, each said IC chip having:
electrical leads extending to one side thereof;
bonding pads disposed at said one side, wherein said bonding pads are electrically connected to said electrical leads;
bumps disposed on said bonding pads, wherein an exposed portion of each of said bumps extends beyond said one side and beyond said bonding pads ...

The Office stated that Frew et al. teaches:

1. "an article comprising a plurality of IC chips 10"
2. "having electrical leads extending to bonding pads on one side of the chip"
3. "bonding pads electrically connected to the electrical leads"
4. "oblong bumps 31 on the bonding pads that extend beyond one side of each chip"
5. "to which the plurality of IC chips are aligned"
6. "and connected to a printed circuit board."

Applicant agrees with points 1-3 and 5-6, but not point 4. The Office's allegation at point 4 contradicts the express language of Frew et al.

Frew et al. discloses a multi-chip circuit module having a plurality of circuit chips assembled in a laminated stack. Each chip includes a layer(s) that comprises a reroute pattern that locates all circuit inputs and outputs pads along a single edge of the chip. Frew et al. explicitly states that the "relocated pads are provided with contact bumps to facilitate the addition of a bonded lead to each I/O pad extending therefrom to a point beyond the edge of each chip." (Col. 1, lines 20-28) Thus, Frew et al. explicitly distinguishes between "bonded leads," which extend beyond the edge of the chip, and bumps, which do not.

In connection with this point, it is notable that Frew et al. does not consider the "bonded leads" to be an inconsequential aspect of its multi-chip module. In particular, Frew et al. distinguishes itself from the prior art, at least in part, based on this feature:

The present invention differs from that of U.S. Pat. No. 5,025,306 in the following respects ...

2. The tape automated bonding (TAB) step for attaching leads to the relocated I/O pads is a step not relevant in the prior invention. The TAB operation is advantageous in that it provides convenient testing of each chip, prior to lamination, thereby avoiding costly errors and reworks.

(Col. 2, lines 26-39)

So, Frew et al. does not disclose

bumps disposed on bonding pads, wherein an exposed portion of each of said bumps extends beyond said one side [of the chip] and beyond said bonding pads ...
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... as recited 16. Consequently, independent claim 16 and claims 17-19 dependent thereon are not anticipated by Frew et al. It is therefore requested that the Office withdraw its Section 102 rejection of claims 16-19 over Frew et al.

Claims 9-15 are Not Obvious
Over the Combination of Ball
and Frew et al.

The Office alleges that Frew et al. teach all of the limitations of claims 9-15 except that "one side of the chip has a foreshortened portion or that adjacent chips in the stack are connected by an epoxy adhesive." The Office finds, however, that Ball "teaches a foreshortened side to allow for bumps while reducing chip stack

thickness to a minimum and epoxy disposal between adjacent chips." The Office alleges that it would have been obvious to use foreshortened sides where bumps are located since it allows "more room for the bumps while maintaining a minimal distance between chips and thus decreases the thickness of the stack and conserve PCB real estate." And so finds the balance of applicant's claims obvious.

Applicant disagrees with the Office's contentions that:

- Ball teaches a foreshortened side;
- A foreshortened side allows for more room for the bumps;
- A foreshortened side decreases the thickness of the stack to conserve PCB real estate.

Independent claim 9 recites, in pertinent part, a chip stack comprising:

a chip stack comprising a plurality of integrated circuit chips ("IC") that are disposed in spaced and parallel relation to one another, each said IC having two major surfaces, four sides, an active device area and a kerf surrounding said active device area, wherein:

at least a portion of said kerf along one of said sides of each IC is removed defining a foreshortened side thereof;

said foreshortened side of said ICs are aligned;
a plurality of bumps are disposed along said foreshortened side between opposing major surfaces of adjacent ICs;

each said bump is disposed partially in said active device area of said IC and partially beyond an edge of said foreshortened side.

Ball discloses an "alternative embodiment" of its stacked semiconductor device wherein, "unlike previous embodiments," the semiconductor substrates are stacked "face-to-back side." To accommodate this, Ball discloses that the periphery of the substrates should include "notches or recesses 910 or chamfers 911 to expose bond pads on lower substrate." The notch has "an opposing pair of walls extending to a terminating wall." (See FIG. 9 and the accompanying disclosure at col. 8, lines 17-31.)

Ball does not teach a "foreshortened side;" he teaches *notching* the side. This approach appears to be useful when chips are stacked with their major surfaces

parallel to the circuit board. In particular, the notches on an upper chip or substrate (902) expose a bond pad (906) on the next lower chip (904), facilitating interconnection.

But the notches of Ball have no use or relevance in conjunction with Frew et al. or applicant's invention, wherein chips are stacked with their major surfaces perpendicular to the circuit board. The notches are of no use since the leads of Frew et al. and the bumps of applicant's invention must extend beyond the furthest edge of the chip to make contact with an underlying circuit board, etc. So the recessed portion of the chip between the two "opposing walls" that define the notch provide no advantage — the leads of Frew et al. would need to extend beyond the opposing walls (that define the notch).

It should be noted that applicant has defined the language "removing at least a portion of said kerf" to mean removing a portion of the width of the kerf for the complete length of the side bearing the bumps. (See, p. 10, ¶ 0063 through p. 11, ¶ 0063.) Claim 9 recites that the side having the portion of the kerf removed is defined as a "foreshortened side." Thus, the term "foreshortened side" means that the full extent of the side is shortened. Therefore, the notched side of Ball does not read on the "foreshortened side" recited in applicant's claims.

Regarding the second point listed above, in the arrangement of Ball, the notches expose the bond pads on the underlying chip so that electrical connection can be made to those underlying bond pads, not to "allow more room for bumps." But in any case, if the notches of Ball were applied to Frew et al. (or the applicant's invention), they would not serve any obvious purpose — and certainly would not "allow more room for bumps" nor facilitate electrical connection.

Finally, foreshortening the side of each chip (10) (along which the leads are arrayed) in the multi-chip stack (30) of Frew et al. does NOT conserve any PCB real estate whatsoever; it simply affects the **height** of the stack above the underlying substrate. (See, e.g., FIGs. 4, 5a and 6.)

Fairly read, there is no suggestion in cited art to apply the teachings of Ball to the multi-chip module of Frew et al., nor would one skilled in the art be otherwise motivated to do so. And even if such a combination were appropriate under patent law, which it is not, when the references are so combined, they still do not yield applicant's invention.

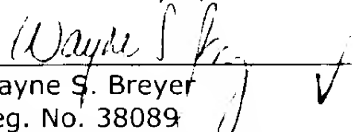
It is submitted, therefore, that claims 9-15 are allowable over the combination of Ball and Frew et al. It is requested that the rejection of these claims is withdrawn.

Conclusion

It is believed that claims 9-19 now presented for examination are in condition for allowance. A notice to that effect is requested.

Respectfully,

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